APPARATUS AND METHOD FOR MARGIN TESTING SINGLE POLYSILICON EEPROM CELLS

Abstract of the Disclosure

Disclosed is a method and apparatus for evaluating margin voltages in single poly EEPROM cells. Briefly, the invention involves shifting the cell's threshold voltage higher, resulting in a corresponding rise in the margin voltage, so that testing for the erase margin may be conducted in the positive voltage range. The present invention implements a variety of solutions to the problem, including both innovations in cell processing and circuitry. In one embodiment, the process steps employed to create the floating gate transistor are changed in order to increase its threshold voltage. Alternatively, or in combination with these general process changes, the width of the floating gate transistor may be reduced, resulting in a corresponding increase in the margin voltage. Circuit modifications include providing a separate test mode condition where the sense amp trip current is higher than under normal operation, and raising the source line's voltage level with a new sense amp optimization, or only during the margin testing mode, both of which shift the erase margin voltages for the cell into the testable range.